

10061475  
02/01/2002

U.S. UTILITY Patent Application

PATENT NUMBER and  
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10061475	02/01/2002	257		2811	<i>Loke</i>

\*\*APPLICANTS: Krutsick Thomas;

\*\*CONTINUING DATA VERIFIED:

*none*  
*Loke*

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\*\* FOREIGN APPLICATIONS VERIFIED:

*none*  
*Loke*

PG-PUB DO NOT PUBLISH ☐

RESCIND ☐

Foreign priority claimed ☐ yes ☒ no

35 USC 119 conditions met ☐ yes ☒ no

Verified and Acknowledged Examiners's initials *Loke*

ATTORNEY DOCKET NO

10

TITLE : Method of fabricating complementary self-aligned bipolar transistors

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Assistant Examiner	Total Claims <input type="checkbox"/> Print Claim for O.G. <input type="checkbox"/>
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg. <input type="checkbox"/> Print Fig. <input type="checkbox"/>
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		Primary Examiner	Application Examiner
		<b>PREPARED FOR ISSUE</b>	
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